Graphene Field Effect Transistors on SiC with T-Shaped Gate: Homogeneity and RF performance

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Abstract

Due to its very high carrier mobility, carrier saturation velocity, large critical current density [1-3], and the ultrathin body allowing channel length scaling without the non-ideal short channel effect [4-5], graphene has attracted enormous attention in recent years for radiofrequency transistor applications for post-silicon electronics [6].

Here we present field effect transistors (FETs) fabricated on a 1/4 of 2-inch graphene wafer where the homogeneity of the GFETS realized across the whole substrate was studied.

Epitaxial graphene is synthesized on semi-insulating 4H-SiC wafers by thermal decomposition. The graphene is grown in a UHV chamber on the Si-face of the substrate at 1150° C under a Si flux. The number of layers and the quality of the graphene are characterized by Raman spectroscopy. As shown in figure (1), the characteristic Raman spectrum of graphene includes a narrow G-peak (1580 cm^{-1}) and a single Lorentzian 2D-peak (2685 cm^{-1}). The number of layers is estimated from the intensities ratio I_{2D}/I_G to be around 4 layers.

Structures for the Hall Effect Measurements were fabricated to measure the Hall mobility μ and the sheet carrier concentration n_s at 300° K in a Bridge configuration. The values of mobility and the sheet carrier concentration are respectively 780 cm^2/v.s and 8.7 10^{+12} /cm^2. The contact and sheet resistivity of the Ni/Au (10nm/40nm) stacking were determined by the Transmission Line Method. The values were extracted from the curve shown in figure 2, $_c$ = 2.1 x 10^{-6} ô /cm^2 and $_{sh}$ = 800 ô /sq.

We fabricated GFETs with a T-shaped gate to reduce the gate access resistance. The fabrication process flow is shown in the schematic diagram of figure (3-a). The graphene was patterned by e-beam lithography. The source and drain contacts of Ni/Au were obtained by e-beam evaporation metal deposition and standard lift-off. After the deposition of 2 nm of Al which was left to oxidize in air, 10 nm of Al_2O_3 were deposited by ALD at 300° C, to be used as a high k gate dielectric. We employed a standard trilayer resist E-beam lithography to realize T-shaped gates. Finally, coplanar accesses were realized. Figure (3-b) shows a scanning electron microscope (SEM) image of a full device and a cross section of a 170 nm T-shaped gate.

The devices were characterized both at DC and microwave frequency. The output characteristics of a graphene FET with L_g = 170 nm and W = 12 μm using are shown in figure (4) and the evolution of the transconductance g_m is shown in figure (5). An output current of 25 mA as well as a transconductance of 2.6 mS are achieved at V_d = 2 V.

The RF performances of our GFET transistors were characterized by measuring S-parameters with a power network analyzer PNA (HP AGILENT 8510C) over the frequency range of 0.05 to 67 GHz under ambient conditions. The calibration of the measurement to the probe tips was performed by using LRRM calibration method. Based on our graphene layer, the typical bias condition are for the gate electrode V_{gs}= -3 V, and for the drain electrode V_{ds}= 3 V since this condition provides g_m= 2.9 mS, as confirmed by DC measurement. Figure 6 presents both of the extrinsic (before de-embedding) and intrinsic (after de-embedding) current gain (H21) and maximum available gain (MAG) frequency response of the same graphene RF transistor measured on DC.

Figures 7 and 8 shows the number of the devices providing f_t and f_{max} in each range of frequency. We can remark that the majority of devices feature frequencies between 21 GHz and 34 GHz for f_t and between 12 GHz and 21 GHz for f_{max} reflecting the homogeneity of our graphene and technological process. An intrinsic cut-off frequency f_t as high as 43 GHz has been obtained and the maximum value of f_{max} is 23 GHz.

References

[1] Novoselov, K. S. et al. Nature, 438 (2005) 197. 200.
[2] Zhang, Y. B., Tan, Y. W., Stormer, H. L. & Kim, Nature, 438 (2005) 201. 204.
[3] Berger, C. et al. Science, 312 (2006) 1191. 1196.
[4] H. Xu, ACS Nano., vol. 5, n°3 (2012) 2340 -2347.
[5] S.-J. Han, IEEE Electron Device Lett., vol. 32 (2011) 812 -814.
[6] Wu et al., Proc. IEEE, vol. 101, no 7 (2013) 1620-1637.
[7] N. Meng, IEEE Transactions on Electron Devices, vol. 58, n°6 (2011) 1594 . 1596
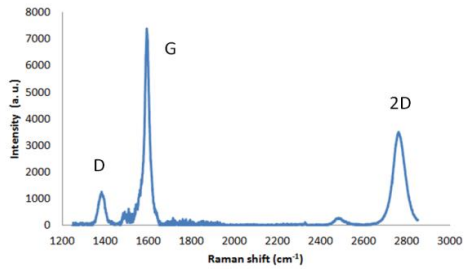
Figures

figure 1 : Raman spectra of Si-face few-layer graphene on SiC showing the G and 2D graphene peaks.
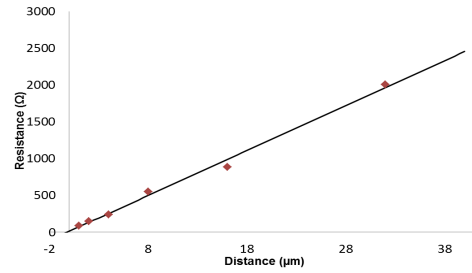

figure 2 : Resistance versus distance R(d) curve for a TLM structure.
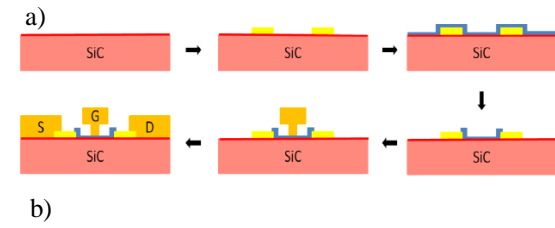

figure 3 : a) process flow for GFET fabrication b) scanning electron microscope (SEM) image of a full device and a cross section of T-shaped gate
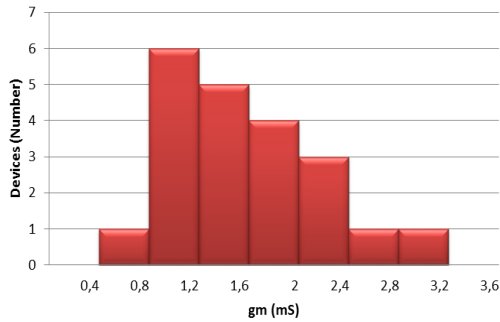

figure 4 : Output characteristics of a graphene FET with L_g= 180 nm and W= 12 µm

figure 5 : Number of devices in each range of g_m transconductences, a value of 2.9 mS has been achieved.

figure 6 : GFET Current and power gain versus frequency for the device with L_g= 170 nm and W= 12 µm Bias point Vgs= -3 V, Vds= 2 V with ft = 33 GHz and f_{max} = 19.5 GHz.

figure 7 : Number of devices in each range of f_{max} frequencies, a maximum oscillation frequency f_{max} of 23 GHz has been obtained.

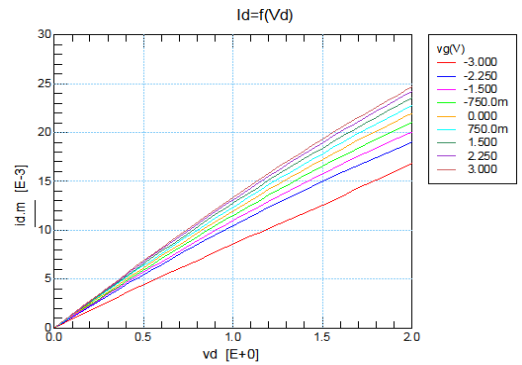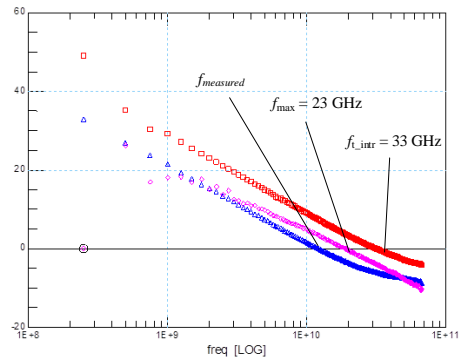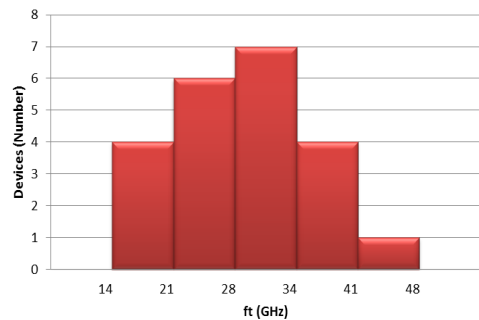figure 8 : Number of devices in each range of f_t frequencies, an intrinsic cut-off frequency f_t of 43 GHz has been obtained